ifelseWare, Inc.

AION ENTERPRISE

ST 2110 GRANDMASTER & OVERLAY PLATFORM

Technical Architecture & Design Reference

Document Version 1.0

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Abstract

This document describes the system architecture, hardware platform, timing chain design, software implementation, and deployment considerations for Aion Enterprise — a 2U rack-mount appliance developed by ifelseWare, Inc. that provides GPS-disciplined IEEE 1588-2008 PTP grandmaster clock functionality and 8-channel simultaneous SMPTE ST 2110 Ultra HD overlay processing within a single integrated system. The document is intended for broadcast engineers, systems architects, and technical evaluators assessing Aion Enterprise for deployment in ST 2110 IP broadcast infrastructure.

1. The ST 2110 Synchronization Problem

SMPTE ST 2110 is a suite of standards governing the transport of uncompressed video, audio, and ancillary data as separate essence streams over managed IP networks. Unlike SDI, where timing is inherent in the serial bitstream, ST 2110 depends entirely on an external timing reference — IEEE 1588-2008 Precision Time Protocol — to maintain synchronization across all devices on the fabric. Without a stable, accurate PTP grandmaster, an ST 2110 network cannot function correctly.

1.1 PTP Grandmaster Requirements

A PTP grandmaster clock is the authoritative time source for an ST 2110 domain. All slave devices — cameras, switchers, routers, capture cards, replay servers — discipline their internal clocks to the grandmaster via the Best Master Clock Algorithm (BMCA). The accuracy requirements are non-trivial:

- **SMPTE ST 2059-2** specifies the PTP profile for professional media networks, requiring grandmaster accuracy sufficient to maintain sample-level alignment across all essence streams.
- **AES67 audio interoperability** requires PTP synchronization to within ± 1 microsecond across all endpoints for seamless audio routing.
- **ST 2110-21 traffic shaping** defines sender timing models (narrow and wide) that depend on accurate PTP lock to remain within compliance bounds.

In practice, this means the grandmaster must be disciplined to an external reference — GPS-derived UTC is the standard for facilities requiring traceability and long-term stability. A GPS-disciplined grandmaster eliminates drift, survives NTP outages, and provides a timing reference that is coherent with wall-clock time, which is essential for any operation that correlates broadcast timing with real-world events.

1.2 The Overlay System Problem

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ST 2110 overlay systems — graphics engines, branding inserters, timecode burners — must themselves be locked to the same PTP reference as the rest of the fabric. An overlay system that is not tightly synchronized to the grandmaster will produce visible timing artifacts: tearing at essence boundaries, audio/video drift, and frame-level inconsistencies that accumulate over time.

Traditionally, grandmaster clock hardware and overlay processing hardware are sourced separately — different vendors, different integration points, different support contracts. The integrator is responsible for ensuring that both are correctly configured within the same PTP domain, that the overlay system's PTP slave is properly disciplined, and that the combined system remains coherent under all operating conditions. This integration burden is non-trivial and represents a significant source of deployment complexity and cost.

> *Aion Enterprise addresses both requirements within a single system. The grandmaster clock and the overlay engine share not only the same PTP domain but the same physical hardware clock — they are architecturally incapable of drifting relative to each other.*

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2. System Architecture

Aion Enterprise is organized around three functional planes that share a common timing reference:

- **Timing Plane:** GPS receiver → PTP Hardware Clock (PHC) → linuxptp grandmaster → dual 10GbE distribution
- **Media Plane:** ST 2110 ingest and egress via dual 100G QSFP28 → CPU-based overlay rendering → LTC embedding in ST 2110-30 audio
- **Management Plane:** IPMI out-of-band management, web-based operator interface, NMOS IS-04/IS-05, system telemetry

The physical separation of the timing/management plane (10GbE) from the media plane (100G) is a deliberate architectural decision consistent with SMPTE recommendations for professional ST 2110 deployments. Media traffic never contends with PTP traffic for network resources, and PTP multicast is confined to the timing plane switches where it can be managed with appropriate QoS policies.

2.1 Timing Chain

2.1.1 GPS Front-End

The GPS front-end consists of a timing-grade GPS receiver connected to an externally mounted active antenna via SMA coaxial connection. This architecture is intentional and differs from the USB-integrated GPS antenna used in the original Aion product, which was designed for mobile deployments where a self-contained form factor takes priority over absolute timing precision.

For Aion Enterprise, which targets permanent or semi-permanent rack installations in facilities and mobile production trucks, the SMA/coax approach is architecturally correct for the following reasons:

- **Antenna placement independence:** The receiver can be located inside the rack while the antenna is roof-mounted, providing reliable sky view regardless of rack room location. Standard low-loss RG-6 or LMR-series coaxial cable is used for the antenna run.
- **1PPS signal integrity:** A hardware serial connection for the 1PPS discipline signal avoids the variable USB interrupt latency that is inherent in USB-connected GPS receivers. USB latency jitter, while typically handled by gpsd's offset correction, introduces unnecessary uncertainty into the PHC discipline loop.
- **Receiver selection:** The SMA interface is compatible with timing-firmware variants of u-blox M8/M9/F9-series receivers, which optimize 1PPS accuracy rather than position accuracy. These receivers provide a configurable 1PPS pulse with sub-100ns accuracy relative to GPS time.

The GPS receiver communicates with the host system via hardware serial, providing NMEA 0183 time sentences to gpsd. The 1PPS hardware signal is connected directly to a GPIO or serial DCD pin to provide the precise timing edge that disciplines the PHC.

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2.1.2 PTP Hardware Clock and PHC Discipline

The system's PTP Hardware Clock (PHC) resides in the network interface controller hardware. linuxptp's `phc2sys` daemon continuously disciplines the Linux system clock to the PHC, and the PHC is in turn disciplined by the GPS 1PPS signal via `gpsd` and the linuxptp servo. This two-stage discipline chain ensures that all software timing — including the overlay timecode generation engine — is coherent with the hardware PTP reference.

The discipline loop operates as follows: `gpsd` parses NMEA sentences for UTC date and TAI-UTC offset, and monitors the 1PPS edge. `ptp4l` references gpsd via the SHM (shared memory) refclock driver, using the 1PPS edge as the precision timing reference. `phc2sys` then disciplines the system CLOCK_REALTIME to the PHC continuously. The result is a system clock that is GPS-traceable to UTC and disciplined to within the sub-microsecond range under normal operating conditions.

> *A known failure mode in PHC-based PTP implementations is incorrect TAI-UTC offset handling, which manifests as a 37-second (currently) error in reported PTP time. Aion Enterprise explicitly sources the TAI-UTC offset from gpsd's NMEA parsing rather than from raw PHC register queries, which do not carry leap second information. This is a design lesson learned during Aion development and is explicitly addressed in the Enterprise implementation.*

2.1.3 PTP Grandmaster Distribution

linuxptp's `ptp4l` operates in grandmaster mode, advertising the system as a Grandmaster-capable clock with a GPS-traceable clock class. PTP announce, sync, and delay request/response messages are distributed over the dual onboard 10GbE interfaces.

The onboard 10GbE network interface controllers support hardware timestamping — the timestamp of outgoing sync messages is captured in hardware at the physical layer rather than in software, eliminating the OS scheduling jitter that would otherwise degrade PTP accuracy. This is a hard requirement for grandmaster-quality PTP distribution; software timestamping is not acceptable for this role.

The dual 10GbE interfaces on the timing plane can be used in two configurations depending on facility network topology:

- **Single-domain distribution:** Both interfaces connect to the same PTP-aware switch fabric, providing link redundancy for the grandmaster connection without requiring SMPTE 2022-7 at the timing plane level.
- **Dual-domain distribution:** Each interface connects to an independent switch, supporting deployments that maintain physically separate primary and secondary timing networks for maximum fault isolation.

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Aion Enterprise implements IEEE 1588-2008 (PTPv2) in grandmaster mode under the SMPTE ST 2059-2 broadcast profile. This is deliberate — ST 2059-2 is defined against the 2008 specification, and every ST 2110 device currently shipping conforms to that profile. IEEE 1588-2019 (PTPv2.1), published in November 2019, introduces backwards-compatible additions to the 2008 standard — primarily security authentication extensions and enhanced profile mechanisms — that do not alter the core synchronization mechanism or the clock hierarchy architecture. Aion Enterprise's hardware-timestamping NICs are fully capable at the physical layer for 1588-2019 operation. As the broadcast ecosystem and SMPTE ST 2059-2 profile adoption of 1588-2019 features matures, support can be extended via linuxptp software updates without hardware changes.

2.2 Media Plane — ST 2110 Processing

2.2.1 ST 2110 Ingest and Egress

The media plane is built around a PCIe Gen 4 IP video capture and playback card providing dual QSFP28 100G Ethernet connections. Each QSFP28 port operates at 100 Gbps full-duplex, providing a combined 200 Gbps of available media bandwidth. This is the foundation for SMPTE 2022-7 seamless protection switching — both ports carry identical traffic simultaneously, and the receiver selects the best packet from either path on a per-packet basis, providing hitless failover if one path fails.

The card supports SMPTE ST 2110-20 (uncompressed video), ST 2110-21 (traffic shaping and flow timing), ST 2110-30 (audio, used for LTC embedding), and ST 2110-40 (ancillary data). Multicast is supported natively, allowing a single transmitted essence stream to be received by multiple downstream devices simultaneously.

Bandwidth analysis for 8 simultaneous UHD channels:

Bandwidth Requirements — 8× UHD 2110-20 Uncompressed		
Format	Per-Channel Bandwidth	8-Channel Total
1080p60 10-bit 4:2:2	~1.5 Gbps	~12 Gbps
2160p30 10-bit 4:2:2	~5.8 Gbps	~46 Gbps
2160p60 10-bit 4:2:2	~11.6 Gbps	~93 Gbps (IP10 codec required)
2160p60 10-bit 4:2:2 (IP10)	~9.0 Gbps est.	~72 Gbps — within 100G budget

At UHD 2160p60, 8 uncompressed channels at full 10-bit 4:2:2 bandwidth would nominally exceed the 100G per-port budget. The IP10 codec — an open standard low-latency codec integrated into the capture card's FPGA — reduces the per-channel data rate with only 8 samples of latency, bringing

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the 8-channel UHD aggregate within the 100G envelope. For 1080p and 2160p30 operation, no compression is required and all channels are carried as fully uncompressed ST 2110-20 flows.

2.2.2 CPU Overlay Pipeline

Overlay rendering is performed on the CPU using the Cairo graphics library. Cairo renders only the pixels within the configured overlay region — the timecode burn-in area — rather than processing the full frame. For a typical broadcast timecode overlay occupying a small fraction of the total frame area, this makes per-channel CPU load modest even at UHD resolution.

The data path for CPU-based overlay processing is:

- Capture card DMA → system RAM → Cairo overlay render → return DMA to capture card → outgoing ST 2110-20 flow

Each overlay channel is processed by an independent high-priority thread with explicit CPU affinity assignment. CPU affinity isolates overlay threads from non-real-time backend processes and prevents OS scheduler interference with frame timing. The i9-14900K's 24 cores provide sufficient parallelism for 8 concurrent overlay threads operating alongside the linuxptp stack, the timecode engine, and the ASP.NET Core backend without resource contention.

2.2.3 LTC Embedding in ST 2110-30

Each of the 8 overlay channels carries its own independently generated LTC (Linear Timecode) value, embedded as an audio signal within that channel's ST 2110-30 essence stream. This approach has several architectural advantages over alternative timecode distribution methods:

- **Essence-coupled delivery:** The timecode travels with the video and audio as a unified ST 2110 flow group. Downstream devices receive the timecode without requiring a separate LTC distribution infrastructure or additional wiring.
- **Independent per-channel values:** Each channel's timecode is generated by an independent software timer instance in the backend. Frame rate, timecode value, and offset are individually configurable per channel, supporting deployments where different channels serve different production contexts or time zones.
- **PTP-coherent generation:** The software timer instances are disciplined to the system clock, which is in turn disciplined to the PHC via phc2sys. The generated timecode values are therefore coherent with the PTP grandmaster reference, ensuring that embedded timecode matches the facility's master time reference.

The LTC signal is generated as a standard audio waveform (bi-phase mark code, SMPTE 12M-2) at the appropriate sample rate for the channel's audio format, then injected into the designated audio channel of the ST 2110-30 flow. Downstream devices that receive the ST 2110 flow can extract the LTC using standard audio decoding, identical to reading LTC from a hardware audio connection.

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3. Hardware Platform

The hardware platform for Aion Enterprise was selected to satisfy three primary requirements: sufficient compute headroom for 8-channel real-time overlay processing alongside the PTP and backend workloads; broadcast-grade reliability through component redundancy and industrial-class power; and compatibility with the PCIe Gen 4 interface requirements of the ST 2110 media card.

3.1 Compute Substrate

The system is built on a server-class Micro-ATX motherboard using the Intel W680 chipset with LGA1700 socket. The W680 chipset is significant because it extends ECC UDIMM support to Intel Core-generation processors — providing the error-correcting memory traditionally associated with Xeon platforms without requiring Xeon hardware pricing or TDP constraints.

The Intel Core i9-14900K provides 24 cores (8 performance + 16 efficiency) with boost clocks up to 6.0 GHz. The selection of the i9-14900K over lower-tier SKUs reflects the CPU-bound nature of the Enterprise workload: with no GPU handling overlay rendering, all 8 concurrent overlay processing threads, the linuxptp grandmaster stack, the timecode engine, the real-time monitoring backend, and NMOS coordination run entirely on the CPU. The i9's additional efficiency cores provide headroom for background tasks without competing with latency-sensitive workloads on the performance cores, a behavior that maps well to the mixed real-time/non-real-time nature of the system. ECC UDIMM support is confirmed on the i9-14900K K-series when paired with the W680 chipset.

The motherboard provides the following interfaces relevant to the Aion Enterprise architecture:

- **PCIe 5.0 ×16:** Primary slot — hosts the ST 2110 capture/playback card. PCIe 5.0 provides 128 GB/s bidirectional bandwidth, well in excess of the 8-lane Gen 4 requirement of the media card, ensuring no bandwidth constraint at the host interface.
- **PCIe 4.0 ×4:** Available for future expansion.
- **Dual 10GbE (Intel X710):** Onboard NICs for the timing and management plane. The X710 controller supports hardware timestamping and is natively supported by linuxptp without driver patches or workarounds.
- **Dual 1GbE (Intel i210):** Onboard NICs for out-of-band management traffic, web UI access, and operator interface connectivity.
- **ASPEED AST2600 BMC:** Provides full IPMI 2.0 remote management independent of host OS state. The BMC has its own dedicated network port and remains operational during host reboots, OS crashes, and firmware updates.

3.2 Overlay Processing Architecture

Aion Enterprise performs all 8-channel overlay processing on the CPU. This is a deliberate architectural decision grounded in measured performance data from the original Aion product line.

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The overlay engine uses Cairo for text rendering. Cairo renders only the pixels within the overlay region rather than reprocessing the full frame, making per-channel CPU load modest even at UHD resolution. On the i9-14900K, 8 concurrent overlay threads running at UHD framerates consume a small fraction of available CPU capacity, leaving substantial headroom for the PTP stack, timecode engine, backend services, and NMOS coordination running concurrently.

Each overlay thread is implemented as a high-priority thread with explicit CPU affinity assignments, isolating real-time overlay workloads from non-real-time backend processes and preventing scheduling interference.

The elimination of a discrete GPU simplifies the chassis architecture in several concrete ways:

- **PCIe slot allocation:** The PCIe 5.0 ×16 primary slot is fully dedicated to the ST 2110 media card with no slot contention.
- **Thermal budget:** Removing a 50–70W GPU TDP from the chassis reduces the total thermal load and simplifies the 2U enclosure cooling design.
- **Power budget:** Total system power draw is reduced, providing additional headroom within the N+1 500W module configuration.
- **Reliability surface:** Fewer active components reduces the number of failure modes in a system expected to operate continuously in production environments.

3.3 Power Subsystem

The power subsystem is an industrial-grade redundant ATX PSU in a 2U form factor, providing two independent 500W modules in an N+1 configuration. Either module can sustain the full system load independently; both operate simultaneously under normal conditions with load sharing.

Hot-swap capability means a failed module can be physically removed and replaced while the system continues operating at full performance on the remaining module. This is a hard requirement for any broadcast appliance where planned maintenance cannot be scheduled during production windows.

The PSU accepts 90–264VAC input across the full range without voltage selection, and operates from 47–63 Hz. This full-range input is relevant for mobile production truck deployments where generator power quality may vary, and for international facilities operating on 50 Hz mains.

3.4 Thermal Management

The i9-14900K's thermal design presents a meaningful challenge in a 2U chassis: the processor's maximum turbo power draw reaches 253W, which exceeds what conventional 2U tower coolers can

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manage within the airflow constraints of a rack-mount enclosure. Aion Enterprise uses the Dynatron L35 — an all-in-one liquid cooler specifically designed for 2U rackmount servers — with a rated Intel TDP ceiling of 305W, providing approximately 50W of thermal headroom above worst-case load.

The L35 uses a copper cold plate attached to the CPU, a 323mm radiator cooled by three 80mm PWM dual ball-bearing fans, and pre-applied Shin-Etsu thermal compound. The radiator mounts within the custom 2U chassis with fan exhaust directed toward the rear of the enclosure. LGA1700 socket compatibility is native.

Liquid cooling in this context provides two operational advantages beyond thermal headroom:

- **Acoustic profile:** A liquid-cooled CPU operates at significantly lower fan speeds than air cooling under sustained load, which is relevant for mobile production environments where rack noise is a consideration.
- **Thermal stability:** Liquid cooling maintains more consistent CPU temperatures under variable workloads, reducing the frequency of thermal throttling events that could affect real-time processing latency on the 8-channel overlay threads.

3.5 Front Panel Diagnostic Display

The front panel carries a 3.5-inch 640×480 IPS DSI display driven by a Raspberry Pi Zero 2W — a dedicated single-board computer physically separate from the main compute platform. This display subsystem is architecturally independent: it has its own processor, its own boot sequence, and its own power rail.

The independence is deliberate. A diagnostic display that depends on the main system's OS or display stack provides no diagnostic value during the events when diagnostic information is most needed — system crashes, kernel panics, boot failures, and firmware updates. The Raspberry Pi Zero 2W communicates with the main backend via USB serial, polling for status data and rendering locally. It continues to display last-known status if the connection is lost, and can display hardware-sourced information independently of the main software stack.

The 3.5-inch form factor was selected to accommodate the Dynatron L35 radiator within the custom 2U chassis front panel — the 304mm radiator occupies the majority of the internal front width, and the compact display integrates cleanly alongside it without compromising either the cooling geometry or the front panel aesthetic.

The display UI is implemented in LVGL (Light and Versatile Graphics Library). Status presented includes PTP lock state and grandmaster stratum, GPS lock and fix quality, per-channel ST 2110 stream health for all 8 channels, 10GbE and 100G link states, CPU thermal readings, and PSU module status.

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4. Timecode Distribution Hub

Aion Enterprise provides six distinct timecode distribution mechanisms, all derived from the same GPS-disciplined UTC reference. This architecture reflects the operational reality of broadcast and live event facilities: a single deployment may simultaneously contain ST 2110 IP devices, legacy SDI-era hardware, lighting consoles, show control systems, and production contexts requiring different time representations — each demanding a different protocol or format.

The six available distribution mechanisms are:

- **PTP grandmaster distribution** via dual 10GbE — the primary reference for all ST 2110 devices on the fabric.
- **ST 2110-30 embedded LTC** — 8 independently managed software timer instances, one per overlay channel, carried inside the IP essence flow.
- **Hardware LTC output** — dedicated LTC generator subprocessor (pure LTC only).
- **Hardware LTC/IRIG A/B output** — dedicated LTC or IRIG A/B generator subprocessor (LTC and IRIG are mutually exclusive on this channel).
- **Art-Net timecode output** and RTC with independent per-channel offsets — for show control systems and multi-timezone or multi-context deployments.
- **Network protocol distribution** — TSL-UMD v5.0 and extended UDP for under-monitor display systems and custom control integration.

All six mechanisms derive their time value from the GPS-disciplined system clock, ensuring mutual coherence across PTP slaves, ST 2110 embedded timecode, hardware LTC and IRIG outputs, Art-Net timecode, network protocol outputs, and RTC offset values. There is no inter-source drift.

4.1 ST 2110-30 Embedded LTC

The primary timecode distribution mechanism for the ST 2110 media plane is LTC embedded as an audio signal in each channel's ST 2110-30 essence stream. Eight independent software timer instances — one per overlay channel — generate an LTC signal that is injected into the designated audio channel of that flow's 2110-30 stream.

Each timer instance is independently configurable for frame rate, timecode value, and offset. This allows different overlay channels to carry different timecode contexts simultaneously — for example, UTC on channels serving broadcast distribution, local time on channels serving in-venue displays, and show time on channels serving production monitoring, all from the same physical appliance. Timecode travels with the video and audio as a unified ST 2110 flow group; no separate LTC distribution infrastructure is required.

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4.2 Hardware LTC and IRIG Subprocessor Architecture

Aion Enterprise uses four dedicated proprietary 600 MHz subprocessors for hardware timecode I/O, each connected to the main system via USB serial. Each subprocessor handles a single, well-defined role — generator or reader, LTC-only or LTC/IRIG. This dedicated architecture eliminates contention between simultaneous read and write operations and provides fully independent signal paths for each function.

The four subprocessors and their roles are:

- **Subprocessor 1 — LTC Generator:** Dedicated hardware LTC output via XLR. Pure LTC generation only; no IRIG capability on this channel. Independently configurable frame rate, timecode value, and offset.
- **Subprocessor 2 — LTC Reader:** Dedicated hardware LTC input via XLR. Accepts incoming LTC for jam-sync reference or concurrent monitoring. Pure LTC only.
- **Subprocessor 3 — LTC/IRIG A/B Generator:** Hardware output configurable as either LTC (XLR) or IRIG A/B (BNC). LTC and IRIG A/B are mutually exclusive on this channel — when IRIG is active, the channel is dedicated to IRIG output. Independently configurable from Subprocessor 1.
- **Subprocessor 4 — LTC/IRIG A/B Reader:** Hardware input configurable as either LTC (XLR) or IRIG A/B (BNC). LTC and IRIG A/B are mutually exclusive on this channel. Accepts incoming LTC or IRIG for jam-sync reference or concurrent monitoring. Independently configurable from Subprocessor 2.

4.2.1 LTC Output Capability

Two independent LTC outputs are available simultaneously: Subprocessor 1 (dedicated LTC) and Subprocessor 3 (when configured for LTC rather than IRIG). Both outputs can generate concurrently to different destinations with different timecode values, frame rates, and offsets. Representative routing scenarios:

- LTC Out 1 → broadcast truck patch panel (UTC, 29.97 NDF) / LTC Out 2 → in-venue show control (show time, 30 DF)
- LTC Out 1 → camera village (local time, 25 fps) / LTC Out 2 → replay server (UTC, 50 fps)
- LTC Out 1 → master control room / LTC Out 2 → remote facility via dedicated circuit

4.2.2 IRIG A/B Output Capability

When Subprocessor 3 is configured for IRIG output, it generates IRIG A or IRIG B timecode via BNC. The channel is exclusively dedicated to IRIG in this mode — LTC output on Subprocessor 3 is not available simultaneously. Subprocessor 1 continues to provide LTC output independently, so a deployment requiring both IRIG and LTC output simultaneously is fully supported: IRIG on Subprocessor 3, LTC on Subprocessor 1.

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4.2.3 LTC and IRIG Input Capability

Two independent hardware inputs are available: Subprocessor 2 (dedicated LTC reader) and Subprocessor 4 (LTC or IRIG A/B reader). Both inputs can operate simultaneously, monitoring independent external sources. When Subprocessor 4 is configured for IRIG input, LTC input on that channel is not available — Subprocessor 2 continues to provide LTC input independently.

Either or both reader inputs can serve as jam-sync references for the backend's internal software timers, providing continuity with existing facility timecode values during transitions from legacy LTC/IRIG infrastructure to ST 2110-embedded LTC.

> *The four-subprocessor hardware timecode architecture in Aion Enterprise replaces the MIDI subsystem present in the original Aion product. MIDI has no role in a dedicated ST 2110 timing and overlay system. The subprocessor resources previously allocated to MIDI are fully reallocated to LTC and IRIG I/O — a net capability increase for the target deployment context.*

4.3 Art-Net Timecode Output

Aion Enterprise outputs timecode over the Art-Net protocol, targeting lighting consoles, show control systems, and any device in the production infrastructure that accepts Art-Net timecode. Art-Net is the de facto standard for DMX-over-IP in live event and theatrical environments, and Art-TimeCode is supported by virtually all professional lighting consoles and show control platforms.

The Art-Net timecode value is sourced from the backend's timecode engine and is coherent with the PTP grandmaster and all other timecode outputs. Art-Net timecode is transmitted on the management plane network interface, keeping it isolated from the ST 2110 media plane.

4.4 TSL-UMD and Extended UDP Network Distribution

Aion Enterprise distributes timecode over the network via two protocols:

- **TSL-UMD v5.0:** Under-monitor display protocol for tally and timecode distribution to TSL-compatible display systems and multiviewers. Carried forward from the original Aion implementation, TSL-UMD output is transmitted on the management plane network interface.
- **Extended UDP:** The Aion UDP control and timecode distribution protocol, extended for Enterprise to accommodate 8-channel configuration, per-channel timecode values, and the additional configuration parameters introduced by the ST 2110 and hardware LTC/IRIG architecture. The Enterprise UDP implementation is a superset of the Aion UDP protocol — existing Aion UDP integrations are structurally compatible with the extended command set.

Both protocols transmit on the management plane network interface and are coherent with all other timecode distribution mechanisms. TSL and UDP distribution allow any networked device or custom

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integration to receive GPS-disciplined timecode without requiring PTP hardware support or physical LTC wiring.

4.5 RTC with Independent Per-Channel Offsets

The backend supports real-time clock output with independently configurable offsets per channel. This mechanism supports deployment scenarios where different outputs require different time representations from the same GPS reference:

- **Multi-timezone facilities:** A broadcast center serving multiple time zones can provide local-time LTC to each regional output without separate timing sources per zone.
- **Show time vs. wall clock:** Live event productions often operate on a show timecode distinct from wall-clock time. The offset mechanism allows show time to be derived from GPS wall-clock time with a configurable offset, maintaining GPS discipline while presenting production-relevant timecode values.
- **International co-productions:** Productions simultaneously serving feeds to multiple countries can provide each feed's LTC channel with the appropriate local offset without additional hardware.

> *All RTC offset values are applied as deterministic arithmetic offsets to the GPS-disciplined system clock. They do not introduce any independent timing source or drift mechanism into the system. An offset of +3 hours is exactly +10,800 seconds from GPS time — it does not accumulate error independently of the GPS reference.*

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5. Software Platform

5.1 Operating System

Aion Enterprise runs a headless Debian Linux deployment. The choice of Debian is deliberate and reflects lessons from the Aion product line:

- **Release stability:** Debian stable releases have multi-year support windows with conservative package update policies, avoiding the kernel and driver churn that can disrupt production systems on rolling-release distributions.
- **linuxptp compatibility:** The linuxptp package and its kernel dependencies (PTP_1588_CLOCK, PHC subsystem) are well-maintained on Debian stable with documented compatibility across the relevant kernel versions.
- **No forced updates:** Debian does not enforce automatic updates. Software versions on a deployed appliance remain stable until explicitly updated by the operator, which is essential for broadcast equipment that may run continuously for months between maintenance windows.
- **Platform independence:** Debian imposes no platform-specific licensing, telemetry, or vendor lock-in. The system can be reimaged, cloned, and deployed on identical hardware without activation servers or license management.

5.2 Backend Service Architecture

The Aion Enterprise backend is a long-running service built on a modern, cross-platform application framework targeting Linux. The backend is responsible for the following subsystems:

5.2.1 PTP Monitoring and Orchestration

The backend monitors the linuxptp stack via `pmc` (PTP Management Client) queries, parsing grandmaster state, clock class, offset from master, path delay, and slave device count. These values are published to the real-time telemetry stream and displayed on both the front panel diagnostic display and the web-based operator interface. Anomalous PTP state — loss of GPS lock, unexpected clock class demotion, excessive offset — triggers alerting through the monitoring subsystem.

5.2.2 Timecode Engine

The timecode engine maintains 8 independent software timer instances, one per overlay channel. Each timer instance tracks a timecode value at the configured frame rate, using the GPS-disciplined system clock as its reference. The engine supports:

- Independent frame rate configuration per channel (23.976, 24, 25, 29.97 DF/NDF, 30, 50, 59.94 DF/NDF, 60)
- Independent timecode value and offset per channel

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- Jam-sync from either hardware LTC reader input (Subprocessor 2 or Subprocessor 4)
- LTC signal generation for embedding into ST 2110-30 audio per channel
- Hardware LTC output generation on Subprocessor 1 (dedicated LTC) and Subprocessor 3 (LTC or IRIG A/B, mutually exclusive)
- Art-Net timecode output for lighting consoles and show control systems
- TSL-UMD v5.0 network timecode distribution
- Extended UDP timecode and control distribution — superset of Aion UDP protocol, extended for 8-channel configuration and Enterprise-specific parameters
- RTC with independently configurable offsets per channel for multi-timezone and multi-context deployments

The timer instances are implemented as high-priority threads with explicit CPU affinity assignments to avoid scheduling interference with the overlay processing threads and the PTP stack.

5.2.3 System Telemetry

Real-time system telemetry is collected by parsing `lm-sensors` output for CPU and board temperature, `top` or `/proc` for CPU and memory utilization, NVMe SMART data for storage health and temperature, and GPIO or I²C reads for PSU module status. All telemetry is published over a real-time push channel to connected operator interfaces, with configurable alert thresholds for each monitored value.

5.2.4 NMOS Coordination

The backend implements NMOS IS-04 (Discovery and Registration) and IS-05 (Connection Management) to allow Aion Enterprise to participate as a fully manageable node in an NMOS-controlled ST 2110 environment. The system advertises its 8 output flows as NMOS senders and any configured input flows as NMOS receivers, allowing a facility's NMOS controller to manage Aion Enterprise's stream routing alongside all other devices on the fabric.

5.2.5 Network Monitor and Async Retry

The backend includes a network monitor service that tracks the link state of all interfaces — both 10GbE timing plane ports and the 100G media plane ports. Link state changes are published to connected interfaces via real-time push notifications. The service implements async DHCP retry logic for interfaces that may not have an address at startup, ensuring that the backend reaches a fully connected state without blocking initialization of timing-critical subsystems.

5.3 Operator Interface

The operator interface is a web-based application served by the backend, accessible from any workstation on the management network without client software installation. Three views are provided:

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- **Time Display View:** Full-screen GPS-locked time display for TOC and control room contexts. Shows UTC time, local time, PTP grandmaster status, and stratum level.
- **TCV Application View:** Timecode verification and monitoring. Real-time status for both LTC reader inputs (Subprocessors 2 and 4), IRIG reader status when active on Subprocessor 4, software timer status for all 8 overlay channels, Art-Net output status, TSL and UDP distribution status, and frame-accurate timing chain monitoring from GPS through to embedded LTC.
- **Enterprise Admin View:** Multi-channel administration interface. Per-channel overlay configuration, ST 2110 stream routing and health status, grandmaster clock dashboard, hardware LTC and IRIG I/O configuration across all four subprocessors, Art-Net configuration, TSL-UMD and UDP configuration, RTC offset management, and full system telemetry panel.

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6. Deployment Considerations

6.1 Network Requirements

Aion Enterprise requires a PTP-aware switched network infrastructure on the timing plane. Specifically:

- **PTP boundary clocks or transparent clocks:** Layer 2 switches between Aion Enterprise and its PTP slaves must either implement IEEE 1588 transparent clock support (to correct residence time) or be PTP boundary clocks. Standard managed switches without PTP support will introduce uncompensated switch delay variability that degrades slave accuracy.
- **IGMP snooping:** The timing plane switch must have IGMP snooping enabled and correctly configured to manage PTP multicast traffic. Without IGMP snooping, PTP multicast floods all ports, consuming bandwidth and potentially interfering with other traffic.
- **QoS / DSCP:** PTP traffic should be marked with appropriate DSCP values (typically CS7 for sync messages) and the switch configured to prioritize these queues over general management traffic.

The media plane (100G) requires QSFP28-capable switches with sufficient backplane capacity for the full 8-channel media load. Standard ST 2110 network design practices apply — leaf-spine topology with non-blocking fabric recommended for multi-source, multi-destination deployments.

6.2 GPS Antenna Installation

The GPS antenna should be mounted with clear sky view — ideally roof-mounted with no obstructions above 10 degrees elevation. Standard active GPS antennas with LNA (low-noise amplifier) are recommended for coaxial runs exceeding 5 meters. Maximum recommended coaxial run length depends on cable type and LNA gain; most antenna manufacturers specify this in their datasheets.

Lightning protection should be considered for any externally mounted antenna. A gas discharge tube (GDT) or similar transient protection device installed at the building entry point is appropriate for permanent installations.

6.3 PTP Domain Planning

Aion Enterprise operates as a grandmaster in a single PTP domain. Facilities with existing PTP infrastructure should plan domain numbers to avoid conflicts. If Aion Enterprise is being introduced into a facility with an existing grandmaster, the Best Master Clock Algorithm will negotiate between them based on clock class, accuracy, and priority values. Aion Enterprise's GPS-disciplined clock will have a clock class of 6 (GPS-traceable to UTC) under normal operating conditions, which will take priority over software-only or NTP-disciplined clocks.

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6.4 Holdover Behavior

In the event of GPS signal loss, Aion Enterprise enters holdover mode. The PHC continues to run from its internal oscillator without GPS discipline. Holdover accuracy degrades over time as a function of the oscillator's frequency stability (expressed as parts-per-million per day). The practical holdover duration before PTP accuracy degrades below ST 2110 requirements depends on the specific oscillator characteristics of the NIC hardware. GPS signal loss is reported immediately via the operator interface, front panel display, and the monitoring telemetry stream.

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7. Product Lineage and Implementation Status

Aion Enterprise is a direct architectural descendant of Aion — a shipping commercial product developed by ifelseWare, Inc. for mobile and small-facility broadcast timing deployments. The following components of the Aion Enterprise implementation are derived from production code that has been tested and deployed in field environments:

- GPS/gpsd integration and TAI-UTC offset handling
- linuxptp grandmaster configuration and pmc-based status monitoring
- phc2sys discipline chain implementation
- LTC/IRIG reader and generator subprocessor firmware (four subprocessors)
- System telemetry collection (lm-sensors, thermal, memory, CPU)
- Real-time push notification architecture for operator interfaces
- Network monitor service with async DHCP retry logic
- Time display and TCV application operator views

Components that are new development for Aion Enterprise and do not have direct Aion lineage include:

- ST 2110 media plane integration (DeckLink IP 100G SDK, NMOS IS-04/IS-05)
- 8-channel CPU overlay pipeline — Cairo-based, 8 independent high-priority threads
- Per-channel LTC embedding in ST 2110-30 audio
- Enterprise Admin View operator interface
- Front panel diagnostic display firmware (LVGL on Raspberry Pi Zero 2W)

> *The GPS implementation in Aion (the predecessor product) uses a USB-integrated antenna appropriate for mobile deployments. Aion Enterprise's SMA/serial GPS front-end represents a deliberate architectural change for the permanent-installation use case, not a modification of the mobile Aion product. Both approaches use the same gpsd integration layer and discipline chain — only the physical GPS interface differs.*

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8. Consolidated Technical Specifications

Compute Platform	
Motherboard	Server-class Micro-ATX, Intel W680 chipset, LGA1700, ASPEED AST2600 BMC (IPMI 2.0)
Processor	Intel Core i9-14900K — 24 cores (8P+16E), up to 6.0 GHz boost; ECC UDIMM support confirmed on W680 platform
Memory	DDR5 ECC UDIMM (W680 ECC support) — error-correcting, non-RDIMM
Storage	NVMe SSD via M.2 PCIe 3.0
PCIe	1× PCIe 5.0 ×16 (ST 2110 media card), 1× PCIe 4.0 ×4, 1× PCIe 3.0 ×1
OS	Debian Linux, headless, hardened deployment
Remote Management	IPMI 2.0 via dedicated BMC port (independent of host OS)
Overlay Processing	CPU-based Cairo overlay engine; 8 independent high-priority threads with explicit CPU affinity; per-channel render isolated from PTP stack and backend services

Timing & Synchronization	
GPS Front-End	Timing-grade serial GPS receiver, SMA antenna connector, external roof-mount active antenna
GPS Protocol	NMEA 0183 time sentences via hardware serial; 1PPS hardware discipline signal
GPS Accuracy	Sub-100 ns 1PPS accuracy (receiver-dependent); UTC-traceable
PTP Implementation	linuxptp ptp4l — IEEE 1588-2008, grandmaster mode, SMPTE ST 2059-2 profile
PHC Discipline	phc2sys continuous discipline of CLOCK_REALTIME to PHC
PTP Distribution NICs	2× Intel X710 10GbE — hardware timestamping, linuxptp native support
PTP Accuracy	Sub-microsecond under normal GPS-locked grandmaster conditions
TAI-UTC Handling	Sourced from gpsd NMEA parsing — leap-second aware
Holdover	PHC oscillator-dependent; GPS loss reported immediately via all monitoring channels
Subprocessor 1	Dedicated LTC generator — LTC output (XLR); independently configurable value, frame rate, offset; pure LTC only
Subprocessor 2	Dedicated LTC reader — LTC input (XLR); jam-sync reference or concurrent monitoring; pure LTC only
Subprocessor 3	LTC/IRIG A/B generator — configurable as LTC output (XLR) or IRIG A/B output (BNC); LTC and IRIG mutually exclusive; independently configurable from Subprocessor 1

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Subprocessor 4	LTC/IRIG A/B reader — configurable as LTC input (XLR) or IRIG A/B input (BNC); LTC and IRIG mutually exclusive; independently configurable from Subprocessor 2
Simultaneous LTC Outputs	Two independent LTC outputs available when Subprocessor 3 is in LTC mode; one LTC output (Subprocessor 1) plus IRIG output (Subprocessor 3) when IRIG is active
Simultaneous LTC Inputs	Two independent LTC inputs available when Subprocessor 4 is in LTC mode; one LTC input (Subprocessor 2) plus IRIG input (Subprocessor 4) when IRIG is active
ST 2110-30 LTC	8 independent software timer instances; LTC embedded in ST 2110-30 audio per channel; independent frame rate, value, and offset per channel
Art-Net Output	Art-Net timecode output for lighting consoles and show control systems; GPS-coherent; transmitted on management plane
TSL-UMD	TSL-UMD v5.0 network timecode distribution; management plane interface
UDP Distribution	Extended Aion UDP protocol; superset of original Aion implementation; accommodates 8-channel configuration, per-channel timecode values, and Enterprise-specific parameters
RTC Offsets	Independent per-channel configurable offsets from GPS reference; supports UTC, local time, show time, custom offset; deterministic — no independent drift

Media Plane — ST 2110	
Card Interface	PCIe Gen 4 ×8, compatible with PCIe 5.0 ×16 slot
Network Interfaces	2× 100G QSFP28 — SMPTE 2022-7 seamless redundancy
Video Channels	8 simultaneous Ultra HD — capture and playback concurrent
Video Standards	SD through UHD; all standards to 2160p60 uncompressed; 2160p120 via IP10 codec
ST 2110 Standards	2110-20 (video), 2110-21 (traffic shaping), 2110-30 (audio/LTC), 2110-40 (ANC)
NMOS	IS-04 discovery and registration, IS-05 connection management
Codecs	Uncompressed 10-bit 4:2:2, IP10 (FPGA-based low-latency), ProRes, DNxHD/DNxHR

Power & Mechanical	
CPU Cooling	Dynatron L35 AIO liquid cooler — 2U rackmount compatible; 305 W Intel TDP rating; 323mm radiator; 3× 80mm PWM dual ball-bearing fans; copper cold plate; LGA1700 native
PSU Type	Industrial redundant ATX, 2U form factor
PSU Modules	2× 500W — N+1 redundancy, hot-swappable
Input Voltage	90–264 VAC full range, 47–63 Hz

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Efficiency	>80% typical at 115 VAC (80 Plus)
Form Factor	2U rackmount, custom enclosure, 19-inch EIA standard
Front Panel Display	3.5-inch 640×480 IPS DSI (Waveshare 33086); Raspberry Pi Zero 2W controller; independent power and USB serial connection to main system; LVGL UI
Operating Temperature	0°C – 40°C
Certifications	CE, FCC, RoHS
Origin	Designed and assembled in the USA

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9. Contact and Availability

Aion Enterprise is currently in pre-release. ifelseWare, Inc. is accepting technical inquiries and early deployment discussions from qualified facilities, systems integrators, and production companies evaluating ST 2110 infrastructure.

Availability	
Status	Pre-release — accepting qualified inquiries
Pricing	Available on request. Aion Enterprise is priced significantly below comparable infrastructure assembled from individual components. Contact ifelseWare for formal quotation.
Support Contract	Annual support contract available. Includes priority response SLA, all firmware updates and feature releases, remote diagnostic assistance, and direct engineering support. Pricing available on request.
Full BOM & Component Specs	Available to qualified integrators under NDA

The full hardware bill of materials and detailed component specifications are available to qualified integrators under NDA. Technical white paper, architecture diagrams, and deployment planning assistance are available on request.

Specifications subject to change without notice. Pre-release product information.

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